REMARKS

Claims 47-52 are pending in this application.

Improper Final Rejection

Applicant objects to the status of this action as final. The Office has inappropriately cited MPEP § 706.07(a) in this regard, stating that Applicant's amendment necessitated the new ground(s) of rejection. This is not the case. Applicant's previous amendments, filed in Amendment B on November 7, 2003, were in response to the Office's first office action of May 7, 2003 and the rejections therein. As stated in selected portions of MPEP § 706.07:

> Before final rejection is in order **a clear issue should be developed** between the examiner and applicant. **[I]in reply to [the first] action the applicant should amend with a view to avoiding all the grounds of rejection and objection.** Switching . . . from one set of references to another by the examiner in rejecting in successive actions claims of substantially the same subject matter, will . . . tend to defeat attaining the goal of reaching a clearly defined issue for an early termination, i.e., either an allowance of the application or a final rejection.
>
> While the rules no longer give to an applicant the right to "amend as often as the examiner presents new references or reasons for rejection," **present practice does not sanction hasty and ill-considered final rejections.** The applicant who is seeking to define his or her invention in claims that will give him or her the patent protection to which he or she is justly entitled **should receive the cooperation of the examiner to that end, and not be prematurely cut off in the prosecution of his or her application.**
>
> The examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal.

In accord with MPEP § 706.07, Applicant has endeavored to clarify the issues related to the present invention in response to the Office's first action. Applicant's amendments in Amendment B were entered in response to the rejections therein to further "define his or her invention in claims that will give him or her the patent

protection to which he or she is justly entitled." In view of the fact that the new rejections are based on a combination of newly cited art, it necessarily follows that the previously submitted amendment successfully overcame the previous rejections.

Therefore, Applicant objects to the status of the immediate action as final.

Obvious-type Double Patenting

Applicant has enclosed herewith a Terminal Disclaimer in accordance with 37 CFR 1.130(b) and 37 CFR 321(c) thereby obviating the obvious-type double patenting rejection of claims 47, 48, and 52 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3, and 11 of United States Patent No. 5,919,302 in view of U.S. Patent No. 5,436,175. Accordingly, Applicant requests the rejection be withdrawn.

Patentability of Amended Claims 47-51 over Nakato et al in view of Park et al.

Claim 47 is directed to a silicon on insulator (hereinafter SOI) structure having a device layer, a single crystal silicon handle wafer, and an insulating layer between the device layer and the handle wafer. According to Claim 47, the device layer comprises an axially symmetric region which is **vacancy dominated and substantially free of agglomerated intrinsic point defects,** and which comprises the central axis and has a radial width of at least about 7.5% of the radius of the device layer.

Nakato et al. (U. S. Patent No. 5,436,175) describe an SOI structure having a device layer, a single crystal silicon handle wafer, and an insulating layer between the device layer and the handle wafer. The Office acknowledges that Nakato et al. do not describe or suggest an SOI structure having a device layer with the characteristic features of claim 47, and relies upon the disclosure of Park et al. (U. S. Patent No. 6,045,610) in an attempt to cure the deficiencies of Nakato et al.

Park et al. is directed to silicon ingots and wafers which are either pure or semi-pure. According to Park et al., there are three types of silicon, Interstitial rich (I),

vacancy rich (V) and pure or perfect (P). Their "pure" wafers include only the pure type material and their "semi-pure" wafers include a vacancy rich region surrounded by pure type material.

It has been asserted that the region described by Park et al. as the vacancy rich region is vacancy dominated and substantially free of agglomerated vacancy defects. (Office Action at page 4 last paragraph). However, Park et al. nowhere describe the "V" region, either explicitly or inherently, as being substantially free of agglomerated intrinsic point defects. In fact, the "V" region identified by Park et al., is explicitly described as being a region which includes vacancy agglomerates (column 3 lines 37-42).

Moreover, Park et al., nowhere describe any region as being **vacancy dominated** and substantially free of agglomerated intrinsic point defects. According to Park et al., their defect free region is described as being the pure or perfect region. Park et al., nowhere describe this pure or perfect region as being vacancy dominated. While Park et al., do not explicitly describe their pure or perfect material as being interstitial dominated material, their preferred test method for identifying such pure material precludes persons skilled in the art from concluding otherwise. That is, their preferred test method for identifying pure material is X-Ray Topography analysis and Lifetime measurements after subjecting the sample to a two step thermal treatment at 800°C for 4 hours and then at 1000°C for 16 hours. This test is commonly referred to as a two-step thermal oxidation treatment whereby oxygen precipitates formed by the thermal treatment are revealed as defects by X-Ray Topography or Lifetime measurements. That is, when subjected to such a test, regions in which oxygen precipitation occurs will appear as defect regions and regions in which no oxygen precipitation occurs will appear as non-defect containing regions. Significantly, it is well established that vacancy dominated silicon precipitates oxygen when subjected to a two step oxygen precipitation heat treatment.[1] Accordingly, the region identified by Park et

al. as pure or perfect, is not a vacancy dominated region, since no precipitates are observed after a two step thermal treatment, and certainly is not the vacancy dominated region substantially free of agglomerated intrinsic point defects as required by claim 47.

In order for the Office to show a *prima facie* case of obviousness, one of the requirements of M.P.E.P. §2143 is that the prior art references teach or suggest all of the claim requirements. Applicant respectfully submits that the Office has failed to meet its burden under this prong as the specific requirements of the pending claim are not taught or suggested by Nakato et al. in combination with Park et al. In particular, claim 47 is patentable over Nakato et al. in view of Park et al., since neither reference, whether considered individually or in combination, describes or suggests and SOI structure having a region which is both vacancy dominated and substantially free of agglomerated intrinsic point defects as required by claim 47.

Claims 48-52 depend from claim 47 and are therefore submitted as patentable for the same reasons discussed above with respect to claim 47.

With specific regard to claim 48, Applicant respectfully submits that the Office's assertion that a wafer formed from an ingot grown by the CZ method must inherently have an oxygen content less that about 13 PPMA is incorrect. On this point, the prior art is replete with examples of CZ wafers with concentrations above 13 PPMA. For example, see Horai et al. (U.S. Pat. No. 6,113,687), which describes how oxygen

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[1] "Simulation of the Point Defect Diffusion and Growth Condition For Defect Free CZ Silicon Crystal," Nakamura et al., Electrochemical Society Proceedings Volume 2002-2, p. 554 (2002). Nakamura et al. subjected an axial slice of a Czochralski grown silicon ingot to a thermal anneal at 780 C for 3 hr and at 1000 C for 16 hr and observed the oxygen precipitation by X-ray topography. Nakamura observed two regions with and without oxygen precipitates between the OSF ring and B-band (a type of agglomerated intrinsic point defect) and state that the boundary between the two regions is the boundary between vacancy dominated material and interstitial dominated material. Oxygen precipitation appears on the vacancy side of the boundary and no oxygen precipitation appears on the interstitial side of the boundary. See page 555 line 32 through page 557 line 12-17.

concentration above and below 8.5×10^{17} atoms/cm^3 (approximately 17 PPMA) affects CZ wafers. (See Col. 6, line 49 - Col. 7, line 12). Also see Tamatsuka et al. (U.S. Pat. No. 6,413,310), which discloses a method that preferably yields a CZ wafer with a "low oxygen concentration" below 18 PPMA. (See, e.g., Col. 11, line 66 - Col. 12, line 5). Therefore, the additional requirement of claim 48 that the device layer have an oxygen content less than about 13 PPMA is **not** an inherent feature of wafers grown by the CZ method. Claim 48 is patentable for this reason, as well as those recited above with regard to claim 47.

Claim 49 is further patentable over the cited references in that claim 49 requires that the handle wafer of the SOI structure have a non-uniform concentration of crystal lattice vacancies with the concentration in the bulk layer being greater than the concentration in the surface layer. According to claim 49, the vacancy profile is such that, if the structure were subjected an oxygen precipitation heat treatment, oxygen precipitates would form in the bulk of the handle wafer and a denuded zone would form in the surface layer of the handle wafer.

None of the cited references disclose or suggest any wafer having a non-uniform vacancy concentration, and certainly do not disclose or suggest the non-uniform vacancy concentration of claim 49. Applicant respectfully submits that the Office's assertion that the formation of crystal lattice vacancies is inherent from the SIMOX process disclosed by Nakato et al. is incorrect. M.P.E.P. §2112 and the references cited therein require that the Office provide a basis in fact and/or technical reasoning to reasonably support the determination that an allegedly inherent characteristic <u>necessarily</u> flows from the teachings of the applied prior art. Nakato et al. teach a method of creating a shallow insulating layer to electrically separate the surface region from the bulk layer of the silicon. This insulating layer is formed by implanting molecular oxygen ions or molecular nitrogen ions at a given depth below the surface region of the silicon. (See Col. 4, lines 4-17). Indeed, the resulting structure has a non-uniform concentration of oxygen precipitates when molecular oxygen ions are implanted

in the silicon. But this feature does not necessarily have any relation to a non-uniform concentration of crystal lattice vacancies, which is a required feature of claim 49.

As discussed in the present application, the non-uniform concentration of crystal lattice vacancies described in claim 49 may be formed by thermally annealing a wafer at a temperature in excess of 1150°C under specific atmospheric conditions, then rapidly cooling the wafer at a rate of at least about 5°C/sec. The thermal anneal described in Nakato et al. will not invariably form any crystal lattice vacancies and, to the extent any form, will not invariably form a non-uniform profile. Significantly, the thermal anneal described in Nakato et al. is carried out at a temperature in the range of 1100°C to 1400°C; as discussed in the present application, crystal lattice vacancies form at temperatures in excess of 1150°C. Therefore, the thermal anneal described in Nakato et al. may not form any vacancies at all if carried out at the lower end of the temperature range taught. Moreover even if the thermal anneal described in Nakato et al. was carried out at temperatures greater than 1150°C, the anneal process would not invariably form a non-uniform vacancy profile. As described in the present application, the process for preparing a non-uniform vacancy profile requires rapidly cooling the annealed wafer. Nakato et al. fail to describe or suggest rapidly cooling their wafer and, in fact, fail to even mention the rate at which their wafer is cooled. Claim 49 is patentable for this reason, as well as those recited above with regard to claim 47.

Claims 50 and 51 further require that the interstitial oxygen concentration profile in the handle wafer has certain characteristics. The Office has made no attempt to provide any basis in fact and/or technical reasoning to reasonably support the determination that these characteristics <u>necessarily</u> flow from the teachings of either Nakamura et al. or Park et al.

Applicant respectfully submits that the Office's assertion that the phrase "such that upon subjecting the silicon wafer to an oxygen precipitation heat treatment . . ." constitutes a product by process limitation is incorrect. This phrase imposes a compositional requirement, not a product by process requirement. More specifically,

the claim requires that the handle wafer have a particular vacancy profile. The two-stage heat treatment is used to merely characterize the claimed vacancy profile, since oxygen precipitates form according to this template. The claim does not require that the product be formed by the process described, but that the process may be used to reveal the character of the claimed vacancy profile. As such, it is not a **product by process** limitation.

Support for the requirement in claim 49 that the handle wafer further comprise a surface layer which comprises a first region of the silicon wafer between the front surface and a distance, D_1, of at least about 10 micrometers can be found in the specification at page 18, line 15 - 28, with the requirement explicitly noted in lines 20-21.

Support for the requirement in claim 51 that the handle wafer further comprise a front surface layer consisting of a first region of the silicon wafer within a distance of no more than about 15 micrometers can be found in the specification at page 17, line 27 to page 18, line 14.

With specific regard to claim 52, the Office has not offered any references that constitute a prime facie case of obviousness. If the Office intended to base the rejection of claim 52 on the same combination of Nakato et al. and Park et al. cited with regard to claim 47, the deficiencies of that combination recited above apply here as well. In particular, claim 52 incorporates the same requirements of claim 47 while increasing the minimum width of the first axially symmetric region to at least about 15% of the radius of the device layer as measured from the central axis towards the circumferential edge. No combination of Nakato et al. and Park et al. disclose these requirements, making claim 52 patentable thereover.

CONCLUSION

In view of the foregoing arguments, Applicant respectfully requests that the Office's rejections of claims 47-52 be withdrawn and a Notice of Allowance be issued for these claims.

A check in the amount of $ 2,010.00 for a five month extension of time is enclosed. The Commissioner is hereby authorized to charge any under payment or credit any over payment to Deposit Account No. 19-1345.

Respectfully submitted,

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*Enclosure